ABSTRACT OF THE DISCLOSURE

A memory merged logic (MML) semiconductor device of NMOS and PMOS dual gate structure including embedded memory of a self-aligned structure and a method of manufacturing the same, wherein in the MML semiconductor device, the memory area including n-type metal oxide semiconductor (NMOS) and p-type metal oxide semiconductor (PMOS) are integrated together, wherein the memory area includes a polycide gate electrode, a hard mask pattern comprised of nitride materials which is formed on the polycide gate electrode, a spacer comprised of nitride materials formed along the sidewall of the polycide gate electrode, and a self-aligned contact which is formed between the adjacent spacers and electrically connected with an impurity implantation region formed on a semiconductor substrate. The logic area includes salicided NMOS and PMOS gate electrodes and salicided source/drain regions, and the height of the polycide gate electrode is smaller than the height of the NMOS and PMOS gate electrodes.